INTRODUCTION OF EUV IN IMEC'S DEVICE PROGRAMS

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imec

OUTLINE

Introduction

N10 Logic

- Gate
- Intermediate Metal2
- Via0

Conclusions

Acknowledgements

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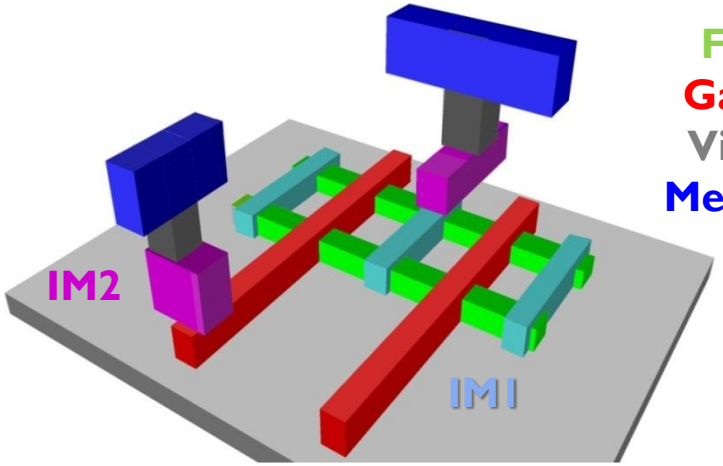
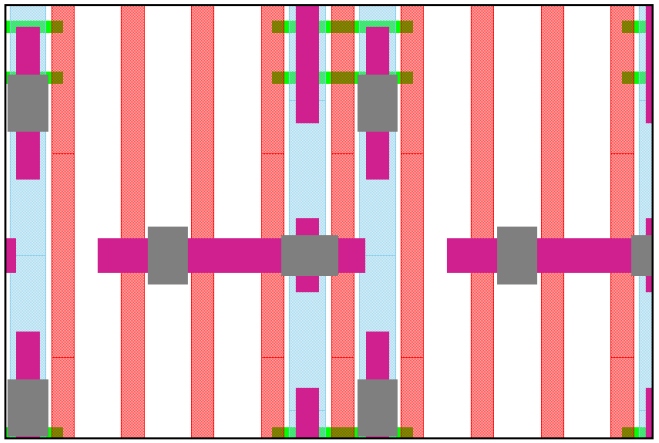
N10 LOGIC ARCHITECTURE



Dual layer Intermediate Metal (IM)

e.g. top-down GDS view on RO



Layer	Vertical		Horizontal	
	CD (nm)	Pitch (nm)	CD (nm)	Pitch (nm)
Active/Fin	-	-	10	45
Gate	20	62	-	-
IM1	22	62	-	-
Gate Open	62	124	53	93
IM2(*)	20/30	62	30/40	80
Via0	40	62	23	45
Metal1	40	62	23	45

(*) Bottom/top CD

LIST OF IMAGING OPTIONS

Layer	# masks 193i	# masks EUV (0.25NA)
Fin/Active		
Gate		
IM1		
GOP		
IM2		
Via0		
Metal1		

LIST OF IMAGING OPTIONS

Layer	# masks	193i	# masks	EUV (0.25NA)
Fin/Active	3	✓		
Gate	3	✓		
IM1	2 or 3	✓		
GOP	1 or 2	✓		
IM2	≥ 3	✓		
Via0	2 or 3	✓		
Metal1	2 or 3	✓		

Ok with multiple patterning !

LIST OF IMAGING OPTIONS

Layer	# masks	193i	# masks	EUV (0.25NA)
Fin/Active	3	✓	3	No clear advantage for EUV
Gate	3	✓	1 or 2	Allows multiple gate lengths
IM1	2 or 3	✓	1 or 2	No clear advantage for EUV
GOP	1 or 2	✓	1	No clear advantage for EUV
IM2	≥ 3	✓	1 or 2	Easier imaging and fewer masks
Via0	2 or 3	✓	1	Easier imaging and fewer masks
Metal1	2 or 3	✓	2	Easier imaging

LIST OF IMAGING OPTIONS

Layer	# masks	193i	# masks	EUV (0.25NA)
Fin/Active	3	✓	3	No clear advantage for EUV
Gate	3	✓	1 or 2	Allows multiple gate lengths
IM1	2 or 3	✓	1 or 2	No clear advantage for EUV
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IM2	≥ 3	✓	1 or 2	Easier imaging and fewer masks
Via0	2 or 3	✓	1	Easier imaging and fewer masks
Metal1	2 or 3	✓	2	Easier imaging

- Focus in this presentation will be on Gate, IM2 and Via0

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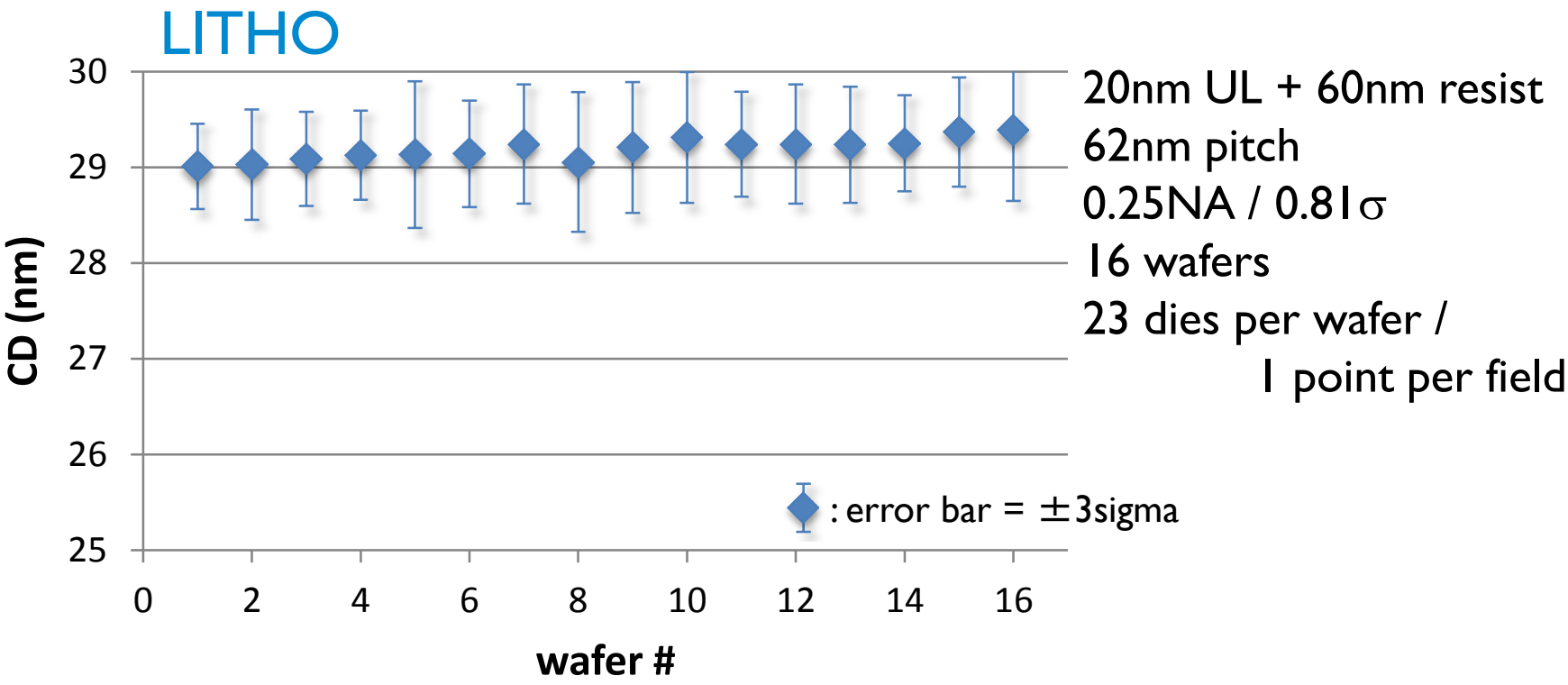
Gate

CD CONTROL THROUGH BATCH



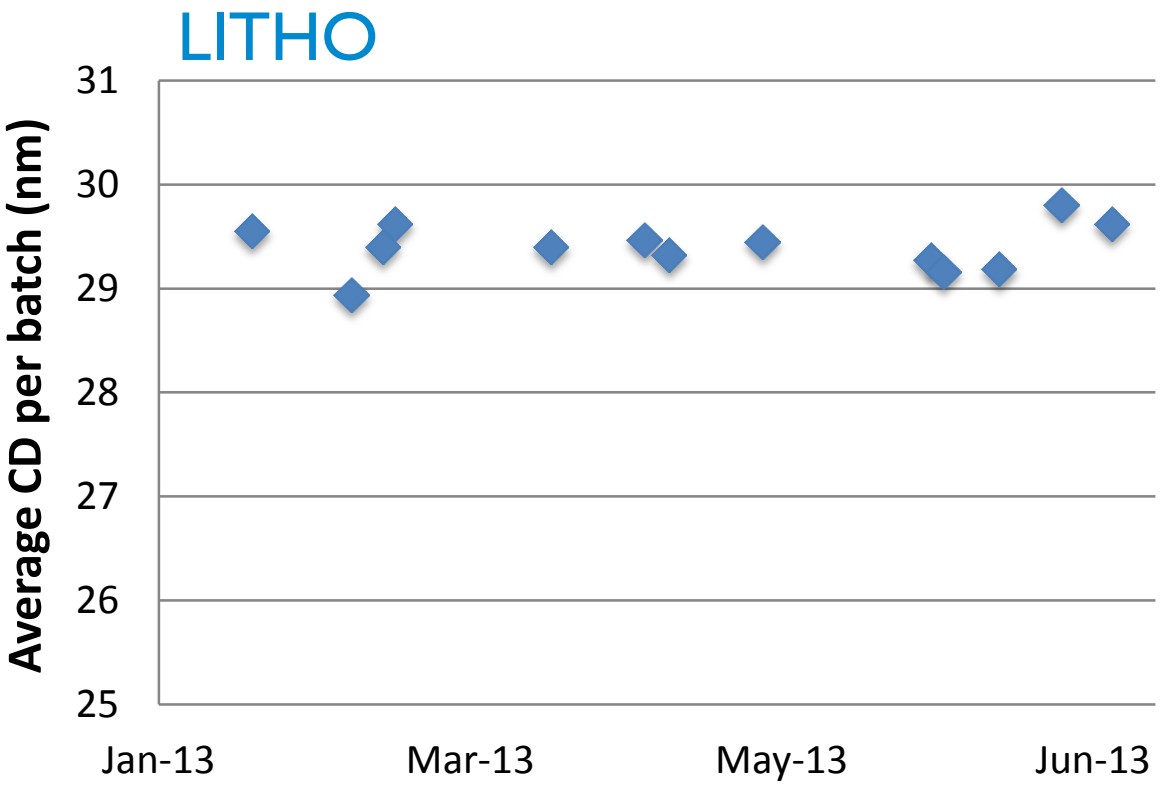
Average CD over batch = 29.2nm

Average intra-wafer 3sigma = 0.6nm

3sigma over batch = 0.7nm

Gate

CD CONTROL OVER TIME



13 lots exposed @ 14mJ.cm^{-2} / 0um
187 wafers in total
all wafers measured

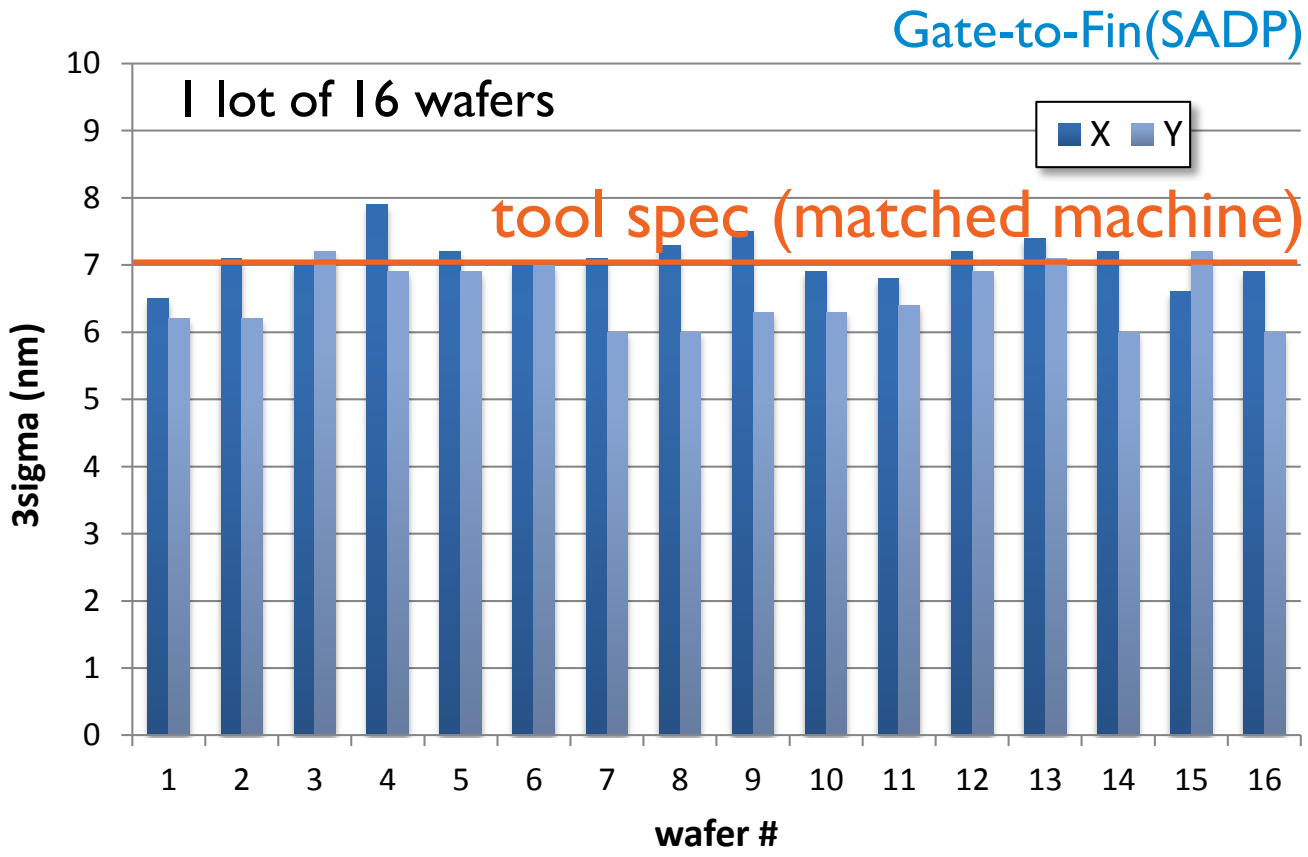
Weighted average CD = 29.3nm

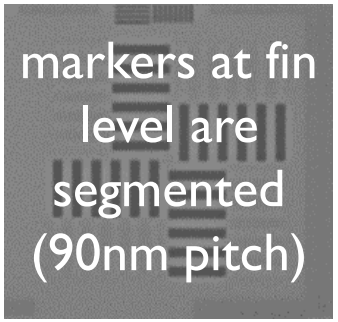
➢ 0.8% variation over 6 months

Gate

OVERLAY CONTROL

MATCHING EUV TO 193i



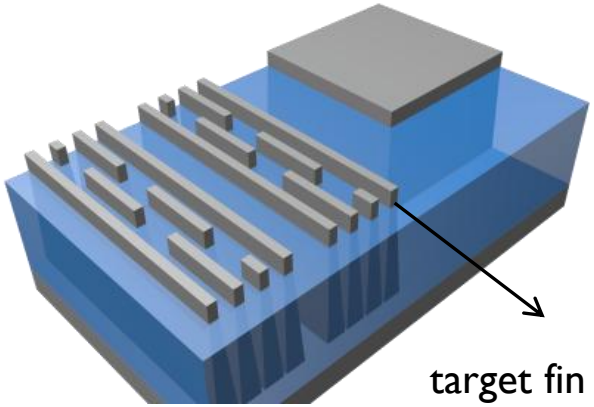


Edge dies excluded, 1point per field for interfield corrections, 5 points per field on 5 dies for intrafield corrections !

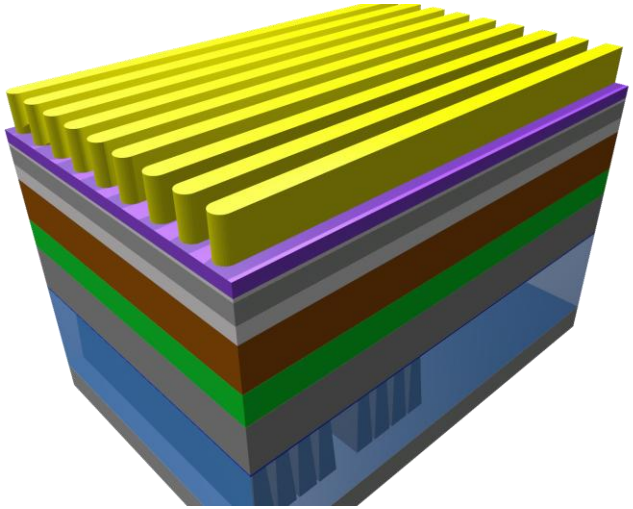
- Applying 10-parameter model on measured overlay, brings residuals down to 6-7nm on product wafer

GATE STACK

62nm pitch



target fin CD = 10nm
and fin height = 30nm



- 60nm resist
- 20nm under-layer
- SiOC
- α-Si

HM patterning + Cut

- SiOC
- α-C
- SiO2 + SiN
- α-Si
- gate oxide
- Fins

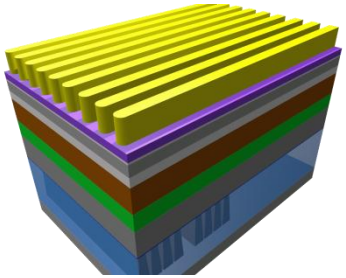
Gate patterning

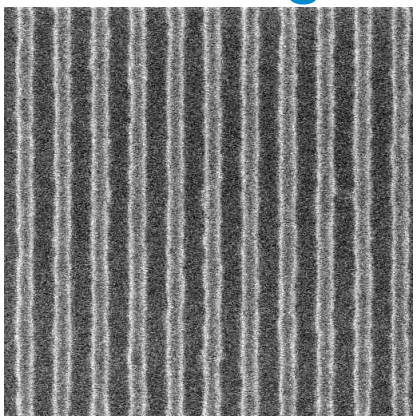
Gate

GATE PATTERNING

GateLine Litho (EUV)

~ 70% brightfield

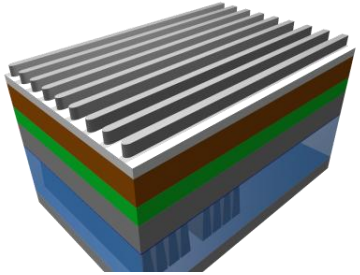


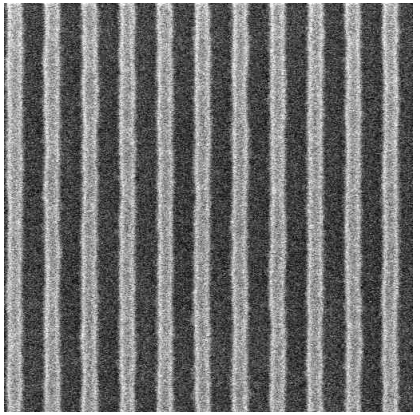


<CD> ≈ 30nm

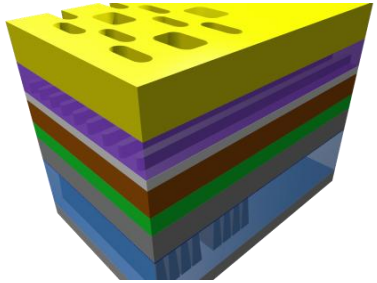
<LWR 3σ> ≈ 4.4nm

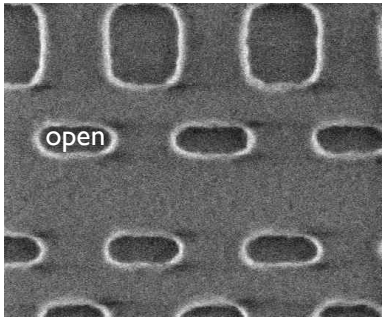
GateLine Etch in HM



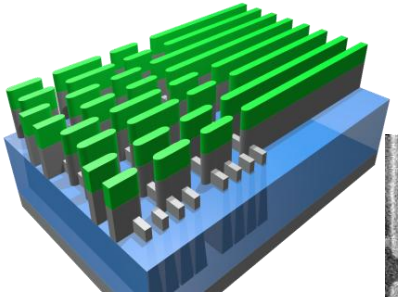


GateCut Litho (193i)



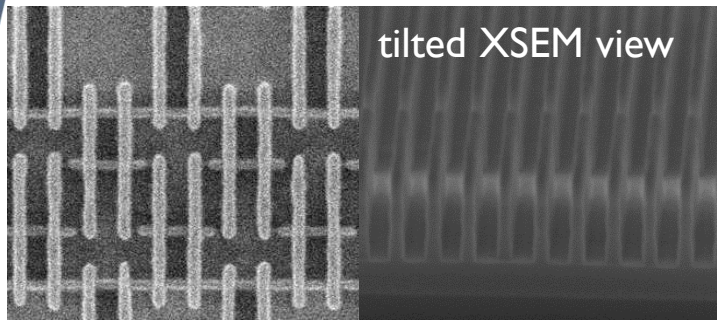


Full Etch



<CD> ≈ 20nm

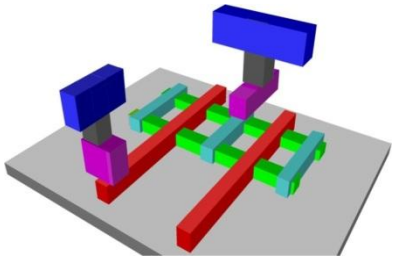
<LWR 3σ> ≈ 4.1nm



aspect ratio ~ 7.5

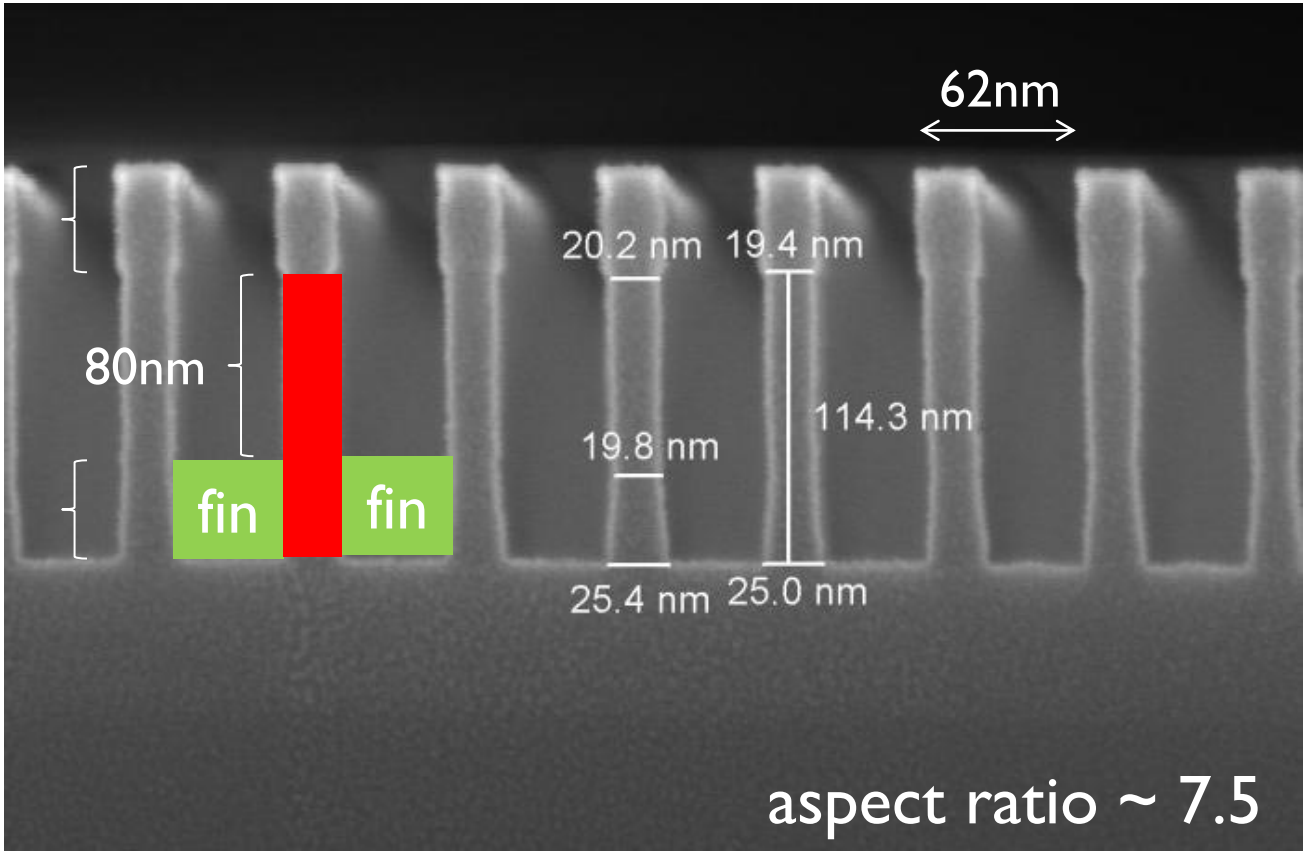
Gate

PROFILE CONTROL AFTER FULL ETCH



Remaining HM

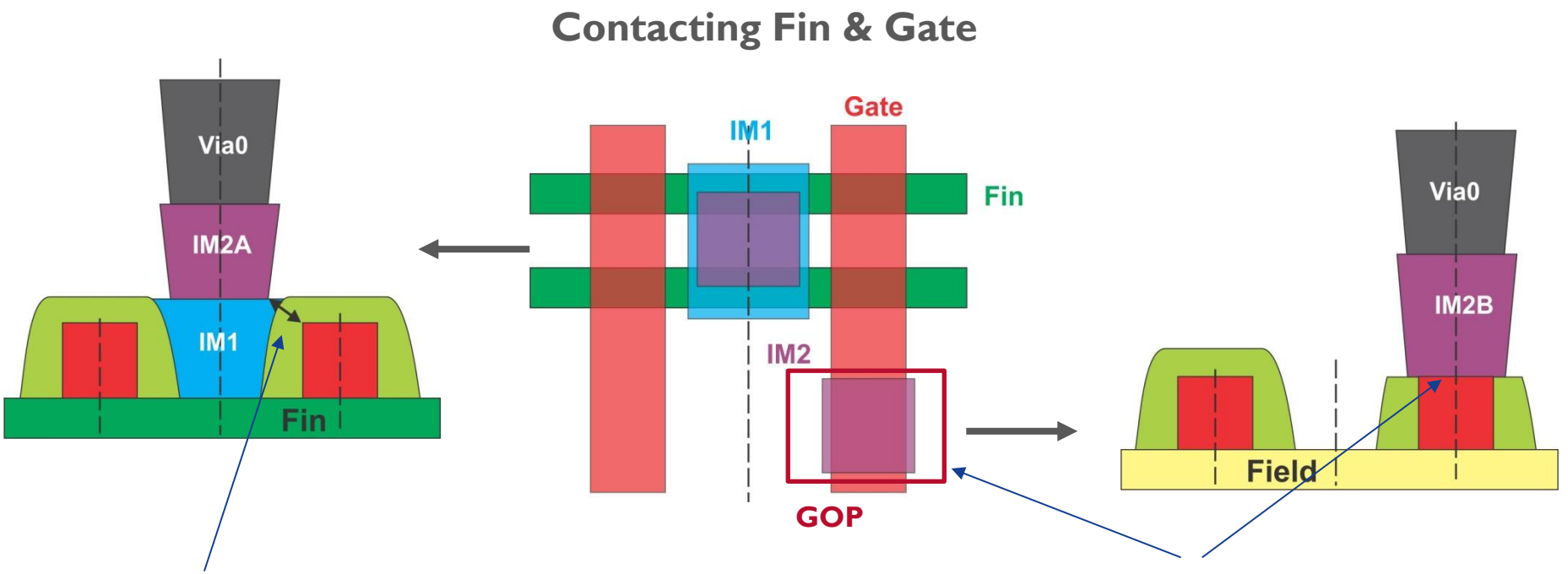
Slight slope during softlanding step



➢ Final fine-tuning of etch recipe currently ongoing

IM2

INTERMEDIATE METAL LAYERS



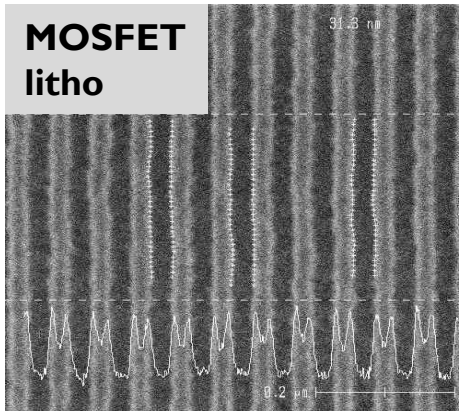
Gate distance is small
Put protective Nitride cap over Gate to avoid short

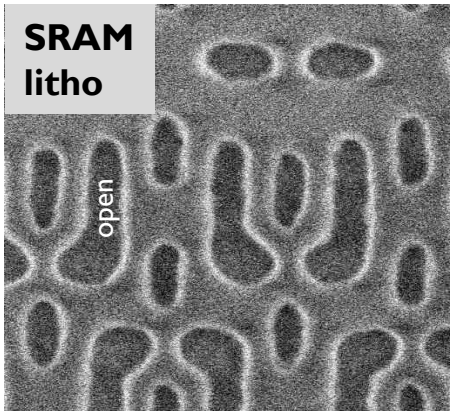
Locally remove this nitride cap where Gate needs to be contacted: "**Gate-Open**" (= extra patterning step)

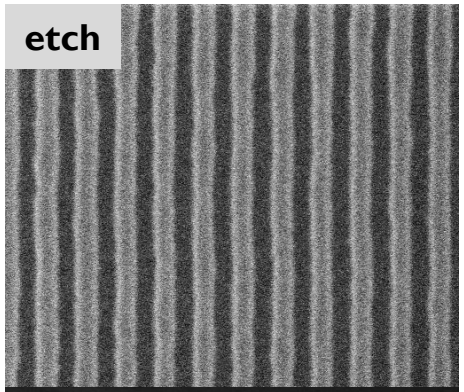
- IM1: contact Active (Fin) – same level as Gate
- IM2: contact Gate & bring Active contacts one level up – one level above Gate
- GOP: protect Gate from shorting to IM2

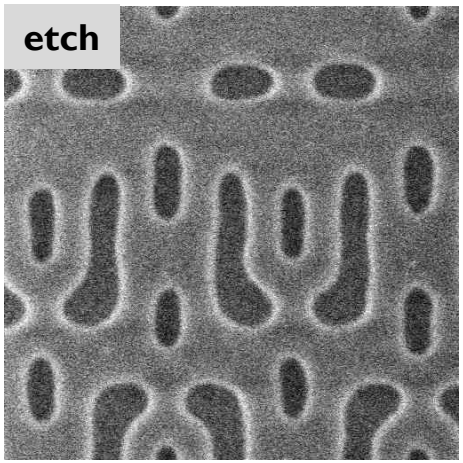
IM2

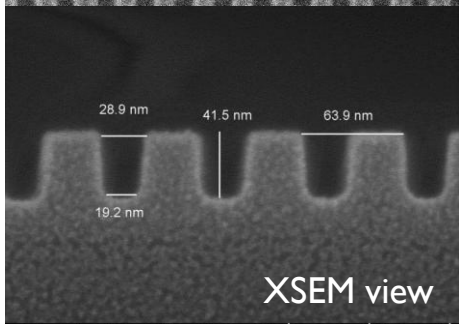
LITHO AND ETCH ON SMALL BATCH











12nm UL + 60nm resist
62nm pitch
0.25NA / 0.81σ
12 wafers
23 dies per wafer

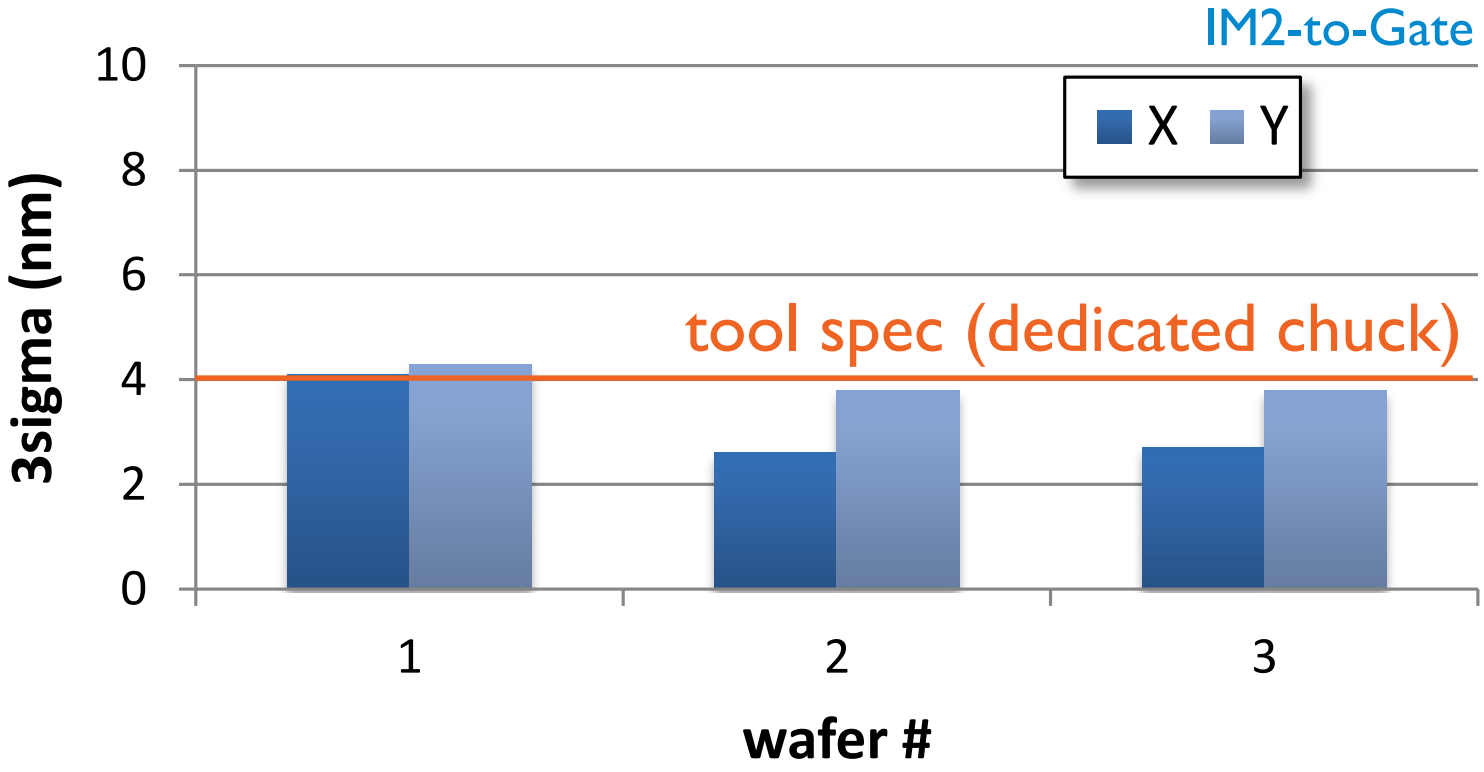
Target	MOSFET Trench M ± 3σ (nm)	SRAM Trench M ± 3σ (nm)
Litho 30nm	31.5 ± 1.6	34.1 ± 5.2
Etch T30/B20nm	27.7 ± 3.1	30.0 ± 4.5

- Acceptable profile performance after etch achieved
- CDU improvement ongoing

IM2

OVERLAY CONTROL

MATCHING EUV TO EUV

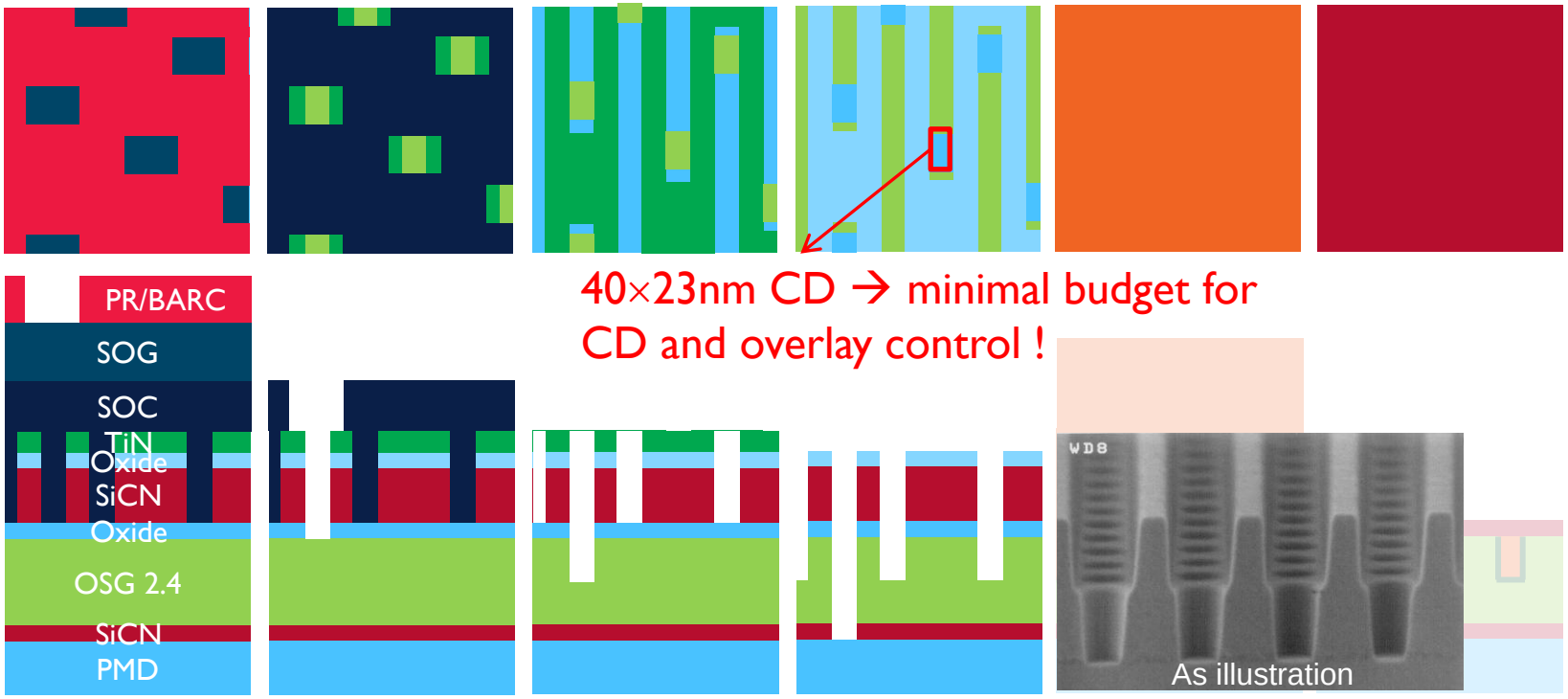


- Applying 10-parameter model on measured overlay, brings residuals down to 3-4nm on product wafer

Via0

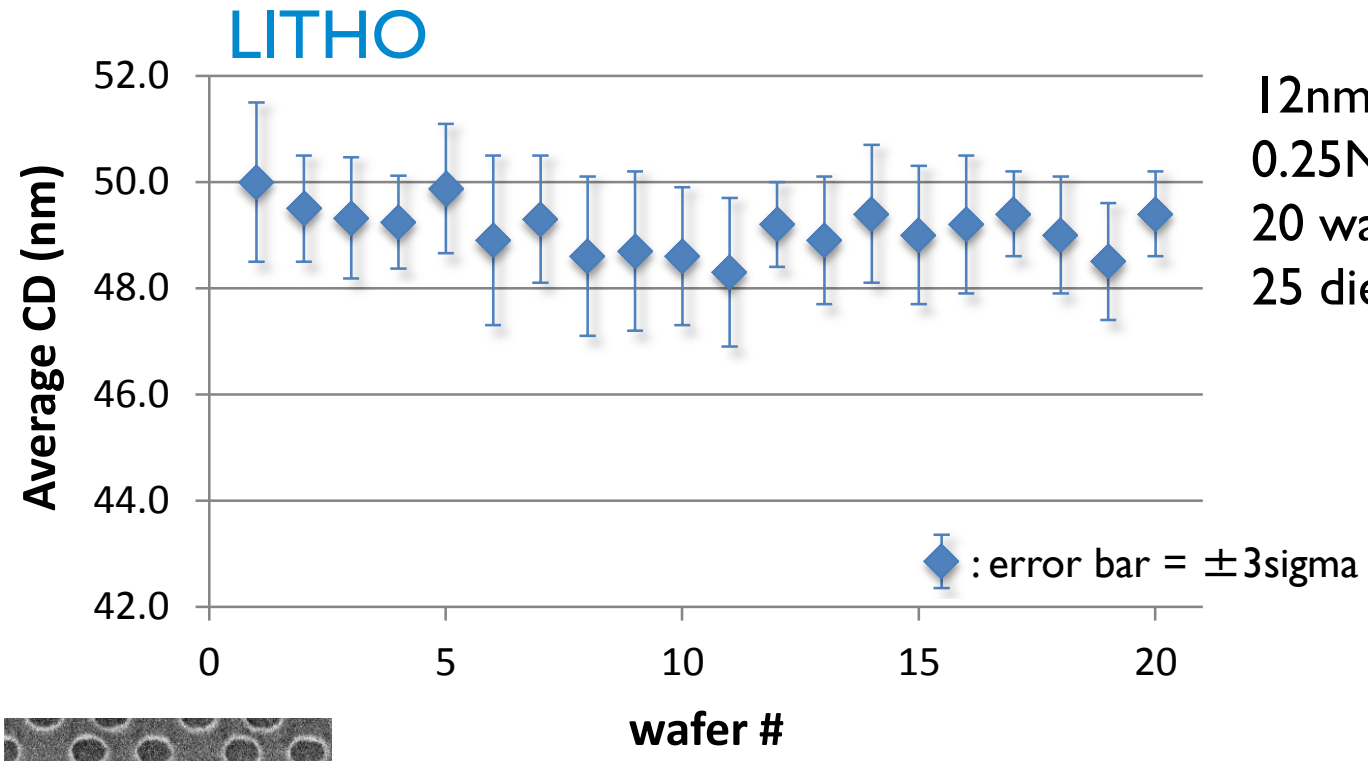
INTRO OF SELF-ALIGNED PATTERNING IN DD MODULE (VIA0/M1)

Partial Trench First approach

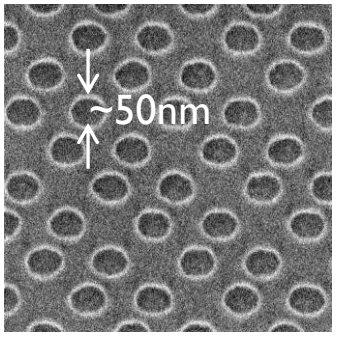


Via0

CD CONTROL THROUGH BATCH



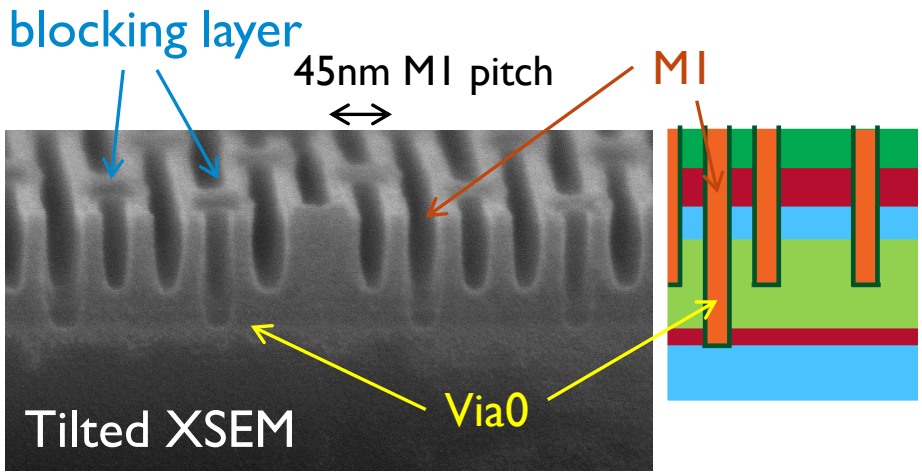
12nm UL + 60nm resist
0.25NA / 0.81σ
20 wafers
25 dies per wafer /
1 point per field



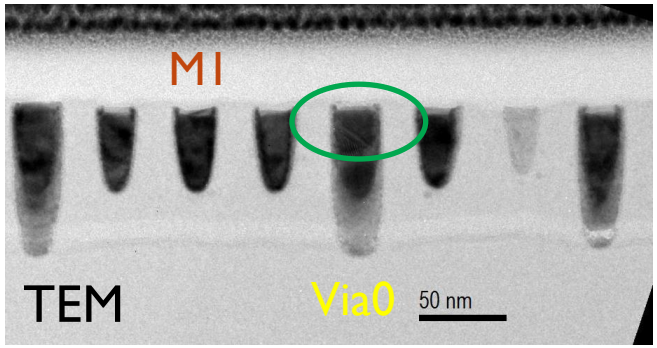
Average CD over batch = 49.1nm
Average intra-wafer 3sigma = 1.2nm

Via0

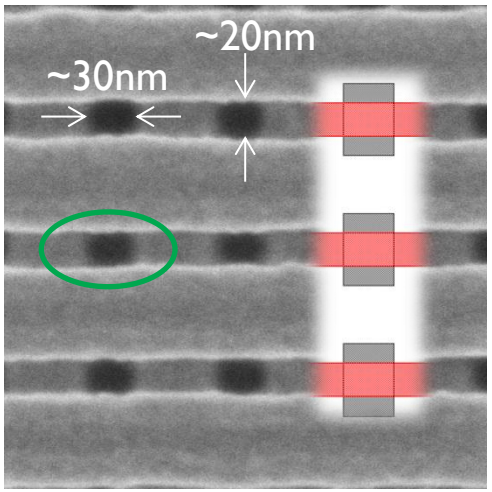
PROOF-OF-CONCEPT

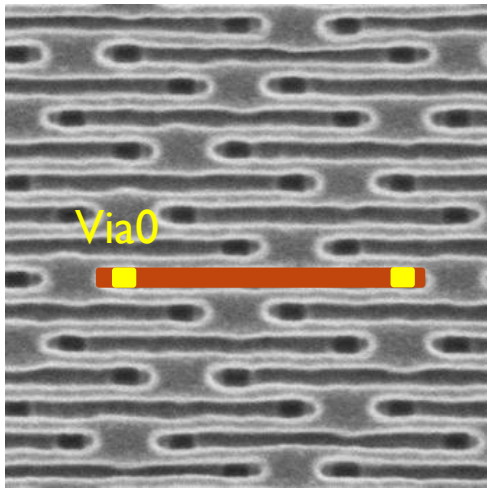


- Self-aligned etch successfully applied
- Within wafer CDU improvement ongoing



Top is not damaged !





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CONCLUSION

Stable litho processing shown through batch and over time

Overlay performance on product wafers meets tool target specifications

EUV litho integrated in N10 Logic Gate, IM2 and Via0 patterning

- Acceptable profile performance achieved after full patterning
- LER/LWR roughness control needs further attention

THANKS TO

all contributors from

- Litho
- Etch
- Thin film deposition
- CMP
- Design & Mask Support
- Respective integration teams
- Material suppliers
- Tool suppliers
- EDA supplier
- Maskshop supplier
- Pilot line support and operations
- ...

THANK YOU !

ASPIRE
INVENT
ACHIEVE

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